REMARKS

Claims 1-7 remain pending in the application.

Claims 1-7 over Weng

In the Office Action, claims 1-7 were rejected under 35 USC 102(b) as allegedly being anticipated by WO 97/23078 to Huang ("Huang"). The Applicants respectfully traverse the rejection.

Claims 1 and 2 recite a single coder/decoder having a **SINGLE** digital/analog conversion channel time division multiplexed among, and a **SINGLE** analog/digital conversion channel concurrently coupled to, a plurality of processors. Claims 3-7 recite time division multiplexing a first plurality of processors to a digital signal input of a single coder/decoder having a SINGLE digital/analog conversion channel, and a SINGLE analog/digital conversion channel, and an analog-to-digital converted signal **concurrently accessible** to **all** of the first plurality of processors.

The Examiner cites col. 8, lines 5-10 of Huang, and particularly Fig. 3a of Huang, for allegedly teaching a single coder/decoder having a digital/analog conversion channel time division multiplexed among, and an analog/digital conversion channel concurrently coupled to, said plurality of processors. (Office Action at 2)

Even a cursory review of Fig. 3a of Huang easily shows that Huange includes a **plurality** of A/D & D/A **conversion** channels within element 13.

The present invention relates to the SHARING of a single codec channel (encoding and decoding) by time division multiplexing in an encoding direction, while concurrently coupling in a decoding direction.

Huang shows nothing more than the use of time division multiplexing to establish a FIXED connection between any processor and an assigned A/D & D/A.

Even if the Examiner were to interpret Huang's use of a time division bus 19 to set FIXED paths between a given A/D & D/A channel at any given time, Huang STILL fails to disclose the present invention. In particular,

Huang would then require **time division multiplexing BOTH** the encoding AND decoding directions to a processor assigned to that time slot. In significant and important distinction from the prior art of Huang, the present invention recites the use of time division multiplexing to a SINGLE D/A conversion channel, while at the same time a SINGLE A/D conversion channel is CONCURRENTLY accessible to ALL processors.

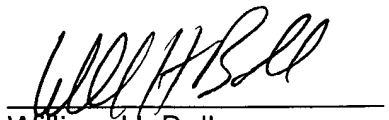
Huang fails to disclose a single coder/decoder having a **SINGLE** digital/analog conversion channel time division multiplexed among, and a **SINGLE** analog/digital conversion channel concurrently coupled to, a plurality of processors as claimed by claims 1 and 2. Huang also fails to disclose time division multiplexing a first plurality of processors to a digital signal input of a single coder/decoder having a SINGLE digital/analog conversion channel, and a SINGLE analog/digital conversion channel, and an analog-to-digital converted signal **concurrently accessible** to **all** of the first plurality of processors, as claimed by claims 3-7.

For these and other reasons, claims 1-7 are patentable over the prior art of record. It is therefore respectfully requested that the rejections be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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